RECORD OF ORAL HEARING

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HIROO NAKANO

Appeal 2007-1984
Application 10/026,813
Technology Center 2100

Oral Hearing Held: October 24, 2007

Before ANITA PELLMAN GROSS, JEAN R. HOMERE, and SCOTT R. BOALICK, *Administrative Patent Judges*.

ON BEHALF OF THE APPELLANT:

OBLON, SPIVAK, MCCLELLAND
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The above-entitled matter came on for hearing on Wednesday, October 24, 2007, commencing at 9:12 a.m., at The U.S. Patent and Trademark Office, 600 Dulany Street, Alexandria, Virginia, before Jennifer M. O'Connor, Notary Public.

JUDGE GROSS: Good morning.

MR. STERN: Good morning, Your Honors.

JUDGE GROSS: You know you have 20 minutes. Whenever you're ready.

MR. STERN: Thank you. As I was introduced, my name is Zachary Stern. I'm from Oblon Spivak and I'm representing Toshiba today in appeal number 2007-1984.

In this case, the applicant is submitting that the references do not teach or suggest each of the features in the claimed invention. Applicant's disclosure describes methods and apparatus for preventing secret information from being extracted from a computer by an unauthorized observer.

The applicants have learned that the current consumption in a computer can be observed by an unauthorized observer and based on peaks and valleys in the current consumption. That unauthorized observer might be able to determine information about what's happening in the computer.

The applicants have discovered that the current is primarily produced by the current drivers driving the data bus between the processor and the memory and therefore, that current occurs primarily during transition times between high and low states being driven on the bus. Applicant's invention is directed to adding a third device to the bus, a pseudo-data generating circuit, and that third device outputs pseudo-data in between read and write cycles so that the transitions between normal data are masked.

Turning to claim one, claim one requires an apparatus that includes three elements that are each connected to the data bus. It requires an operation processing unit, a memory and a pseudo-data generating circuit.

Each of those are connected to the bus. The operating processing unit reads and writes data during read and write cycle periods and the pseudo-data generating circuit outputs pseudo-data to the data bus at time intervals between the read and write cycles.

In the office action, the Examiner applied the reference by *Ugon,* or *Ugon,* to describe the conventional features of a CPU and a memory operating in a computer system. For example, on figure 1 of *Ugon*, the Examiner points out that *Ugon* shows -- and I'll quote from the office action -- "an operating processing unit as item one, a memory, as referred to in column 5, lines 62 to 65, and a data bus, either data bus three or four, in Ugon's Figure 1."

The office action also says that *Ugon* describes a pseudo-data generating circuit connected to the data bus and the office action asserts that column 11, lines 14 through 18 of *Ugon* teaches that feature.

Finally, the office action asserts that the pseudo-data generating circuit generates pseudo-data, but the office action doesn't assert that the pseudo-data generating circuit outputs the pseudo-data to the data bus; it merely asserts that it outputs pseudo-data to said memory to cause instructions to randomly execute.

If we turn to what *Ugon* actually says in the cited passage, *Ugon* refers to three different registers. They're shown in figure 1 as R1, R2 and R3, and in the passage of *Ugon* that's been cited by the Examiner, *Ugon* indicates that R1 is a random generator that can produce random numbers, and that can be used to initialize a timer R3.

The timer R3 can also be initialized by a non-volatile memory 13 and alternatively, the random generator can load information into a registered

R2. In other words, R1 is a random generator that can transfer data to a timer or to a register R2, but *Ugon* doesn't anywhere indicate that the random generator outputs data to the data bus. It only describes situations in which the registers 1, 2 and 3 receive data from the data bus and then in turn, those registers are used to interrupt the processor 15.

There is another connection shown between R1, R2 and R3 and the interrupt 15, but there's no indication that those registers communicate on the data bus. Also, the Examiner did not assert that the random generator outputs data to the data bus. To supply the features lacking in the disclosure of *Ugon*, the Examiner turns to *Feyt*. Just to summarize, in *Ugon*, *Ugon* fails to teach or suggest two features in the claims.

JUDGE HOMERE: Counselor, I have a question for you. In figure 1 here of *Ugon*, when you look at items 10 through -- let's see, one, 11, 12, 13, 14, right, you see there's a data bus three here and then you have arrows going to those devices. In your opinion, where does the information come from to communicate to those devices?

MR. STERN: Your Honor, it appears that the devices in *Ugon* 11 through 13 and 14 are connected to a data bus as in a conventional computer system, so those devices would be transferring data to and from the CPU and in between one another perhaps, although *Ugon* doesn't --

JUDGE HOMERE: Apparently it seems that you're saying that interrupt 15 is not communicating with the other port, those devices that are pointed out, yet you're saying that the CPU itself is sending information to those devices. I want to know why the CPU is communicating with your devices whereas the interrupt is not, the number 15 is not?

MR. STERN: I'm sorry if I didn't make myself clear, Your Honor. What I'm saying is that the random generator R1 doesn't output data to the data bus. There's no indication in *Ugon* that the random generator R1 outputs data to the data bus, nor does the Examiner assert that it does.

The random generator R1 communicates with the timer R3, presumably through the lines connecting them and to have the timer R3 generate an interrupt to the interrupt controller 15. The data bus, as in the claims, is something that connects the CPU and the memory, so that, for example, in *Ugon* could be the item labeled three.

The item labeled three, which does connect to registers R1, R2 and R3 -- however there's no indication in *Ugon* that the random generator R1 outputs pseudo-data to the data bus three. The Examiner doesn't assert that it does either. The Examiner relies on *Feyt* for that.

JUDGE BOALICK: Mr. Stern?

MR. STERN: Yes.

JUDGE BOALICK: I have a question. Assuming we agree with you on the interrupt not communicating with the bus, could you tell me what your position is on the secondary processor disclosed by *Ugon* -- item number two -- that communicates with a dummy RAM, say 21 or 22, and why that would not be a pseudo-data generating circuit?

MR. STERN: Your Honor, that's a different direction than the Examiner asserted, so I'm not sure that it would be fair for me to respond to that. It seems like a new line of argument or rejection. However, I assume from my reading of *Ugon* that the CPU number two and the other memories also operate as conventional memories and they communicate according to data bus four.

JUDGE BOALICK: Thank you.

MR. STERN: If we can turn now to *Feyt*, the office action asserts that *Feyt* "discloses a method for hiding operation performed by the microprocessor card by presenting random data items on the data bus during cryptographic calculations." Then the Examiner goes on to say, the cryptographic calculations require reading and writing operations to be performed by the processor.

The Examiner notes that *Feyt* recites a microprocessor, which in the claims refers to an operation processing unit. The office action indicates that *Feyt* recites a microprocessor that presents random data. The office action also notes that *Feyt* includes a random signal generator in Figure 1, reference number 28. The office action indicates that the random signal generator is used to provide randomness to the power consumption of the processor and memory so that power analysis cannot properly occur.

In each of the embodiments of *Feyt*, the random signal generator 28, which is part of a device 20, is not connected to the data bus that connects the central unit to the memory. Again, *Feyt* also doesn't teach or suggest a pseudo-data generating circuit that is connected to the data bus.

Are there any other questions?

JUDGE GROSS: No, I guess that's it.

MR. STERN: Okay, thank you very much.

JUDGE GROSS: Thank you. Have a good day.

MR. STERN: Thank you.

(Whereupon, at 9:23 a.m., the proceedings were concluded.)